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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/755,742	01/12/2004	Gregory William Smaus	5500-90300	1112

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EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/755,742	SMAUS ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on May 19, 2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Arguments

2. In response to the last Office Action, no claims have been cancelled, amended or added. Claims 1-18 remain pending in this application.

3. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US PGPub No. 20050125613) and Beardsley et al (US Patent No. 6,345,295).

For claim 1, Kim discloses a processor (a computer system includes a central processing unit, par. 0014) comprising:

a trace generator configured to generate a plurality of traces each including one or more operations, wherein one or more operations are decoded from one or more instructions, wherein each of said one or more operations is associated with a respective address (a fill unit forms traces from instructions received from an instruction cache, and a trace cache store instruction traces, where a trace is a set of dynamically formed, logically contiguous decoded-instruction blocks, par. 0019); and

a trace cache memory coupled to said trace generator, wherein said trace cache memory includes a plurality of entries each configured to store one of said plurality of traces (an index is used to allocate entries in trace cache structures instead of a part of the fetch address of the trace; entries that are accessed using temporal indexes are named temporal trace cache entries, par. 0027).

Despite these teachings, Kim does not disclose the remaining claim limitations. Beardsley, however, discloses restricting each of a plurality of traces includes only operations having respective addresses that fall within one or more predetermined ranges of contiguous addresses (an address filter will select and conduct traces for addresses of any of the devices, and alternatively, if a number of devices have contiguous address ranges, a trace tool control may operate the address filter to select fewer address ranges, col. 4, lines 24-31).

Kim and Beardsley are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been

obvious to a person of ordinary skill in the art at the time of the invention to include an address filter for restricting traces because this would allow for selecting different extents of data (col. 4, lines 57-58), as taught by Beardsley.

For claim 10, the combined teachings of Kim and Beardsley disclose the invention as per rejection of claim 1 above.

These teachings further help disclose a method comprising:

generating a trace including one or more operations decoded from one or more instructions, wherein each of said one or more operations is associated with a respective address (Kim: par. 0019, 0027);

storing said trace in a trace cache entry within a trace cache memory (Kim: par. 0019);

restricting said trace to include only operations having respective addresses that fall within one or more predetermined ranges of contiguous addresses (Beardsley: col. 4, lines 24-31).

6. Claims 2-3 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US PGPub No. 20050125613), Beardsley et al (US Patent No. 6,345,295) and Cherian et al (US Patent No. 5,930,497).

For claim 2, the combined teachings of Kim and Beardsley disclose the invention as per rejection of claim 1 above. These teachings fail, however, to disclose the limitations of claim 2.

Cherian, however, discloses a starting address of one or more predetermined ranges of contiguous addresses is based upon the respective address of a given one or more operations within a plurality of traces (an address trace is maintained for each process initialized by the starting address in an associated region of contiguous addresses, col. 8, lines 48-58).

Kim, Beardsley and Cherian are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a starting address of a range of addresses to be based on trace operations because this would allow for tracking activity (col. 9, line 48), state definition, and a specification of events, conditions, outcomes (col. 8, lines 63-65), as taught by Cherian.

For claim 3, Kim and Beardsley disclose the invention as per rejection of claim 1 above.

These teachings fail to disclose the limitations of claim 3.

Cherian, however, helps disclose a starting address of said one or more predetermined ranges of contiguous addresses is based upon said respective address of a first operation of said one or more operations within each of said plurality of traces (col. 8, lines 48-58).

Kim, Beardsley and Cherian are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a starting address of a range of addresses to be based on trace operations because this

would allow for tracking activity (col. 9, line 48), state definition, and a specification of events, conditions, outcomes (col. 8, lines 63-65), as taught by Cherian.

For claim 11, Kim and Beardsley disclose the invention as per rejection of claim 10 above.

These teachings fail to disclose the limitations of claim 11.

Cherian, however, helps disclose a starting address of said one or more predetermined ranges of contiguous addresses is based upon said respective address of a given one of said one or more operations within said trace (col. 8, lines 48-58).

Kim, Beardsley and Cherian are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a starting address of a range of addresses to be based on trace operations because this would allow for tracking activity (col. 9, line 48), state definition, and a specification of events, conditions, outcomes (col. 8, lines 63-65), as taught by Cherian.

For claim 12, Kim and Beardsley disclose the invention as per rejection of claim 10 above.

These teachings fail to disclose the limitations of claim 12.

Cherian, however, helps disclose a starting address of said one or more predetermined ranges of contiguous addresses is based upon said respective address of a first operation of said one or more operations within said trace (col. 8, lines 48-58).

Kim, Beardsley and Cherian are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been

obvious to a person of ordinary skill in the art at the time of the invention to include a starting address of a range of addresses to be based on trace operations because this would allow for tracking activity (col. 9, line 48), state definition, and a specification of events, conditions, outcomes (col. 8, lines 63-65), as taught by Cherian.

7. Claims 4-6 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US PGPub No. 20050125613), Beardsley et al (US Patent No. 6,345,295), Cherian et al (US Patent No. 5,930,497) and Arsenault et al (US Patent No. 6,578,128).

For claim 4, the combined teachings of Kim, Beardsley and Cherian disclose the invention as per the rejection of claim 2 above. These teachings fail, however, to disclose the limitations of claim 4.

Arsenault, however, discloses each of one or more predetermined ranges of contiguous addresses is separated by a predetermined number of contiguous addresses (a memory with a plurality of contiguous memory regions, a plurality of processors, each associated with a corresponding one of the memory regions, and each providing a plurality of sets of processor addresses, and a translator for mapping addresses fed thereto from the processors into the memory addresses, and a gap of addresses separating the last used address in a set from a first used address in a next successive set of addresses, col. 3, lines 65-67 and col. 4, lines 1-12).

Kim, Beardsley, Cherian and Arsenault are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would

have been obvious to a person of ordinary skill in the art at the time of the invention to include ranges of contiguous addresses and a separation thereof because this allows each CPU to write into or read from its designated memory region, and only read data from appropriate memory regions (col. 8, lines 62-66), as taught by Arsenault.

For claim 5, the combined teachings of Kim, Beardsley and Cherian disclose the invention as per rejection of claim 2 above.

These teachings fail to disclose the limitations of claim 5.

Arsenault, however, discloses said one or more predetermined ranges of contiguous addresses includes a first range of contiguous addresses as determined by said respective address of a given one of said one or more operations and a next N sequential ranges of contiguous addresses, where N is any number (col. 3, lines 65-67 and col. 4, lines 1-12).

Kim, Beardsley, Cherian and Arsenault are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include ranges of contiguous addresses and a separation thereof because this allows each CPU to write into or read from its designated memory region, and only read data from appropriate memory regions (col. 8, lines 62-66), as taught by Arsenault.

For claim 6, the combined teachings of Kim, Beardsley and Cherian disclose the invention as per rejection of claim 2 above.

These teachings fail to disclose the limitations of claim 6.

Arsenault, however, discloses said one or more predetermined ranges of contiguous addresses includes a first range of contiguous addresses as determined by said respective address of a given one of said one or more operations and a next sequential range of contiguous addresses (col. 3, lines 65-67 and col. 4, lines 1-12).

Kim, Beardsley, Cherian and Arsenault are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include ranges of contiguous addresses and a separation thereof because this allows each CPU to write into or read from its designated memory region, and only read data from appropriate memory regions (col. 8, lines 62-66), as taught by Arsenault.

For claim 13, the combined teachings of Kim, Beardsley and Cherian disclose the invention as per rejection of claim 11 above.

These teachings fail to disclose the limitations of claim 13.

Arsenault, however, discloses each of said one or more predetermined ranges of contiguous addresses is separated by a predetermined number of contiguous addresses (col. 3, lines 65-67 and col. 4, lines 1-12).

Kim, Beardsley, Cherian and Arsenault are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include ranges of contiguous addresses and a separation thereof because this allows each CPU to write into or read from its designated memory region, and only read data from appropriate memory regions (col. 8, lines 62-66), as taught by Arsenault.

For claim 14, the combined teachings of Kim, Beardsley and Cherian disclose the invention as per rejection of claim 11 above.

These teachings fail to disclose the limitations of claim 14.

Arsenault, however, discloses said one or more predetermined ranges of contiguous addresses includes a first range of contiguous addresses as determined by said respective address of a given one of said one or more operations and a next N sequential ranges of contiguous addresses, where N is any number (col. 3, lines 65-67 and col. 4, lines 1-12).

Kim, Beardsley, Cherian and Arsenault are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include ranges of contiguous addresses and a separation thereof because this allows each CPU to write into or read from its designated memory region, and only read data from appropriate memory regions (col. 8, lines 62-66), as taught by Arsenault.

For claim 15, the combined teachings of Kim, Beardsley and Cherian disclose the invention as per rejection of claim 11 above.

These teachings fail to disclose the limitations of claim 15.

Arsenault, however, discloses said one or more predetermined ranges of contiguous addresses includes a first range of contiguous addresses as determined by said respective address of a given one of said one or more operations and a next sequential range of contiguous addresses (col. 3, lines 65-67 and col. 4, lines 1-12).

Kim, Beardsley, Cherian and Arsenault are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include ranges of contiguous addresses and a separation thereof because this allows each CPU to write into or read from its designated memory region, and only read data from appropriate memory regions (col. 8, lines 62-66), as taught by Arsenault.

8. Claims 7-9 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US PGPub No. 20050125613), Beardsley et al (US Patent No. 6,345,295) and Hughes (US Patent No. 6,973,543).

For claim 7, the combined teachings of Kim and Beardsley disclose the invention as per rejection of claim 1 above. These teachings fail, however, to disclose the limitations of claim 7.

Hughes, however, discloses a trace cache control unit coupled to said trace cache memory and configured to receive a trace cache probe and to store in a trace cache probe storage, an address corresponding to said trace cache probe until said trace cache probe completes (a memory configured to store an indication of one or more addresses, wherein the memory is coupled to receive a first address of a read command, and a control circuit coupled to the memory is configured to cause an issuance of one or more probes corresponding to the read command responsive to the first address missing in the memory, and inhibit the issuance of one or more probes

corresponding to the read command responsive to the first address hitting in the memory, col. 2, lines 17-26).

Kim, Beardsley and Hughes are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a trace cache probe and storage thereof because this would maintain coherency of cache data (col. 2, line 10), and by inhibiting probes appropriately, system bandwidth which would be consumed by the probes may be conserved (col. 1, lines 66-67), as taught by Hughes.

For claim 8, the combined teachings of Kim, Beardsley and Hughes disclose the invention as per rejection of claim 7 above.

These teachings further help disclose said trace cache control unit is further configured to determine whether a trace cache probe to a particular address is outstanding in response to receiving a trace cache fetch to said particular address by comparing said particular address to said address corresponding to said trace cache probe stored within said trace cache probe storage (Kim: par. 0019, 0027; Beardsley: col. 4, lines 24-31; Hughes: col. 2, lines 17-26).

For claim 9, the combined teachings of Kim, Beardsley and Hughes disclose the invention as per rejection of claim 8 above.

Beardsley further helps disclose said trace cache control unit is further configured to block said trace cache fetch in response to determining that said trace cache probe to a particular address is outstanding (a trace stop command may be

provided to one of the trace tools, and the address trace tool stops the trace at its address filter and trace buffer, and issues a breakpoint signal on the breakpoint connection to all the interconnected trace tools, col. 2, lines 10-14).

Kim, Beardsley and Hughes are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include block or stop a trace cache fetch because this would ensure that trace entries will not be overwritten and are saved for analysis (col. 9, lines 7-8), as taught by Beardsley.

For claim 16, the combined teachings of Kim and Beardsley disclose the invention as per rejection of claim 10 above.

These teachings fail to disclose the limitations of claim 16.

Hughes, however, helps disclose receiving a trace cache probe and storing in a trace cache probe storage, an address corresponding to said trace cache probe until said trace cache probe completes (col. 2, lines 17-26).

Kim, Beardsley and Hughes are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a trace cache probe and storage thereof because this would maintain coherency of cache data (col. 2, line 10), and by inhibiting probes appropriately, system bandwidth which would be consumed by the probes may be conserved (col. 1, lines 66-67), as taught by Hughes.

For claim 17, the combined teachings of Kim, Beardsley and Hughes disclose the invention as per rejection of claim 10 above.

These teachings further help disclose in response to receiving a trace cache fetch to a particular address, determining whether a trace cache probe to said particular address is outstanding by comparing said particular address to said address corresponding to said trace cache probe stored within said trace cache probe storage (Kim: par. 0019, 0027; Beardsley: col. 4, lines 24-31; Hughes: col. 2, lines 17-26).

For claim 18, the combined teachings of Kim, Beardsley and Hughes disclose the invention as per rejection of claim 17 above.

Beardsley further helps disclose blocking said trace cache fetch in response to determining that said trace cache probe to a particular address is outstanding (col. 2, lines 10-14).

Citation of Pertinent Prior Art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Groeschel (US PGPub No. 20040216091) discloses memory allocation trace data is analyzed by generating a sorted address index containing records of memory allocations, deallocations, and memory address inquiries.

Bala (US Patent No. 6,233,678) discloses collecting a branch history value of a program executing in a processor, and a current start address register latches a program count value in response to a trace termination condition.

Ayers (US Patent No. 5,210,843) discloses a pseudo set-associative memory caching arrangement with a plurality of cache memory banks each comprising a respective number of addressable locations individually defined by a cache address.

Mann (US Patent No. 6,167,536) discloses an on-chip instruction trace cache capable of providing information for reconstructing instruction execution flow.

Contact Information

10. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 10:00am-6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, is also reachable at 571-272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

8-31-06

SANJIV SHAH
PRIMARY EXAMINER